



## **WIZTECH AUTOMATION SOLUTIONS (P) LTD.,**

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### **Syllabus for Diploma in VLSI Front End Design FPGA DESIGN**

- ❖ FPGA Fundamentals
- ❖ Digital Electronics

#### **VHDL**

- ❖ VHDL Overview and Concepts
- ❖ Levels of Abstraction
- ❖ Entity, Architecture
- ❖ Data Types and declaration
- ❖ Enumerated Data Types
- ❖ Relational, Logical, Arithmetic Operators
- ❖ Signal and Variables, Constants
- ❖ Process Statement
- ❖ Concurrent Statements
- ❖ When-else, With-select
- ❖ Sequential Statement
- ❖ If-then-else, Case
- ❖ Slicing and Concatenation
- ❖ Loop Statements
- ❖ Delta Delay Concept
- ❖ Arrays, Memory Modeling, FSM
- ❖ Writing Procedures
- ❖ Writing Functions
- ❖ Behavioral / RTL Coding
- ❖ Operator Overloading
- ❖ Structural Coding
- ❖ Component declarations and installations

- ❖ Generate Statement
- ❖ Configuration Block
- ❖ Libraries, Standard packages
- ❖ Local and Global Declarations
- ❖ Package, Package body
- ❖ Writing Test Benches
- ❖ Assertion based verification
- ❖ Files read and write operations
- ❖ Code for complex FPGA and ASICs
- ❖ Generics and Generic maps

## **VERILOG**

- ❖ Language introduction
- ❖ Levels of abstraction
- ❖ Module, Ports types and declarations
- ❖ Registers and nets, Arrays
- ❖ Identifiers, Parameters
- ❖ Relational, Arithmetic, Logical, Bit-wise shift Operators
- ❖ Writing expressions
- ❖ Behavioral Modeling
- ❖ Structural Coding
- ❖ Continuous Assignments
- ❖ Procedural Statements
- ❖ Always, Initial Blocks, begin end, fork join
- ❖ Blocking and Non-blocking statements
- ❖ Operation Control Statements
- ❖ If, case
- ❖ Loops: while, for-loop, for-each, repeat
- ❖ Combination and sequential circuit designs
- ❖ Memory modeling,, state machines
- ❖ CMOS gate modeling
- ❖ Writing Tasks
- ❖ Writing Functions
- ❖ Compiler directives
- ❖ Conditional Compilation
- ❖ System Tasks
- ❖ Gate level primitives
- ❖ User defined primitives
- ❖ Delays, Specify block
- ❖ Testbenches, modeling, timing checks
- ❖ Assertion based verification
- ❖ Code for synthesis
- ❖ Advanced topics
- ❖ Writing reusable code

## **FPGA Flow**

- ❖ Re-configurable Devices, FPGA's/CPLD's
- ❖ Architectures of XILINX Device
- ❖ Designing with FPGAs
- ❖ FPGA's and its Design Flows
- ❖ Architecture based coding
- ❖ Efficient resource utilization
- ❖ Constrains based synthesis
- ❖ False paths and multi cycle paths
- ❖ UCF file creation
- ❖ Timing analysis/Floor Planning
- ❖ Place and route/RPM
- ❖ Back annotation, Gate level simulation, SDF Format
- ❖ DSP on FPGA
- ❖ Writing Scripts
- ❖ Hands on experience with industry Standard Tools

## **Duration**

- ❖ FPGA Design + VHDL + FPGA Flow = 45 Days
- ❖ FPGA Design + Verilog + FPGA Flow = 45 Days
- ❖ FPGA Design +VHDL+ Verilog + FPGA Flow =90 Days